Amendments to the Claims

1. (Amend) An output driving circuit comprising:

a first level shifter for receiving an input signal to be provided to an outside of an integrated circuit and shifting a voltage level of the input signal to a voltage level required at the outside of the integrated circuit while maintaining a duty ratio of the ~~input~~ output signal constant;

a second level shifter for receiving an output enable signal, and shifting a voltage level of the output enable signal to a voltage level required at the outside of the integrated circuit while maintaining a duty ratio of the output enable signal constant; and

an output driving unit for forwarding the ~~input~~ output signal to the outside of the integrated circuit under the control of the output enable signal from the second level shifter~~,~~.

wherein the first or second level shifter comprises:

an input signal splitting unit for providing the input signal in two signals having the same delay time periods;

a sense amplifier for amplifying voltage levels of the two signals into a voltage level required at the outside of the integrated circuit; and

a delay compensating unit for making delay time periods of the two signals amplified at the sense amplifier to be the same, and forwarding the two signals, selectively, and

wherein the input signal splitting unit comprises:

first and second inverters for delaying the input signal for a preset time period and providing to one side input terminal of the sense amplifier, and

a first transmission gate for delaying a signal from the first inverter for a time period the same with a delay time period at the second inverter, and providing to the other side input terminal of the sense amplifier.

2-3 (Cancel)

4. (Amend) The output driving circuit as claimed in claim ~~2~~1, wherein the sense amplifier ~~includes~~ comprises a first PMOS transistor and a first NMOS transistor,

and a second PMOS transistor and a second NMOS transistor, respectively connected in series between a power terminal the voltage level required at the outside of the integrated circuit is applied thereto and ground, for providing the voltage level of the power terminal and the voltage level of the ground, selectively.

5. (Amend) The output driving circuit as claimed in claim 4, wherein the first NMOS transistor ~~includes~~ comprises a gate connected to ~~the~~ a second inverter, and serves as a first input terminal, and the second NMOS transistor ~~includes~~ comprises a gate connected to the first transmission gate in the input signal splitting unit, and serves as a second input terminal.

6. (Original) The output driving circuit as claimed in claim 4, wherein the first PMOS transistor includes a gate connected to a connecting point of the second PMOS transistor and the second PMOS transistor, and the connecting point serving as the first output terminal of the sense amplifier, and

the second PMOS transistor includes a gate connected to a connecting point of the first PMOS transistor and a first NMOS transistor, the connecting point serving as the second output terminal.

7. (Amend) The output driving circuit as claimed in claim ~~2~~1, wherein the delay compensating unit ~~includes~~ comprises a ~~third~~ PMOS transistor and a ~~third~~ NMOS transistor connected in series between the power terminal the voltage level required at the outside of the integrated circuit is applied thereto and ground, for providing the voltage level of the power terminal, and the voltage level of the ground, selectively.

8. (Amend) The output driving circuit as claimed in claim 7, wherein the third PMOS transistor includes a gate connected to the first output terminal of the sense amplifier through a third inverter and a second transmission gate,

the ~~third~~ NMOS transistor includes a gate connected to the second output terminal of the sense amplifier through fourth and fifth inverters in succession, and

a connecting point of the ~~third~~ PMOS transistor and the ~~third~~ NMOS transistor connected to the output driving unit through the sixth inverter.

9-16 (Withdrawn)

17. (Original) The output driving circuit as claimed in claim 1, wherein the output driving unit includes;

an NAND gate for receiving for receiving signals from the first level shifter and the second level shifter, subjecting to NAND operation, and providing to a gate of the PMOS transistor,

an NOR gate for receiving signals from the first level shifter and the second level shifter, subjecting to NOR operation, and providing to a gate of the NMOS transistor,

a ninth inverter for receiving, inverting, and providing a signal from the second level shifter to the NAND gate, and

a seventh PMOS transistor and a seventh NMOS transistor connected in series between the power terminal and ground.